

FIG.1

EVENT BASIS FORMAT	
5ns	PIN P1:1 , PIN P2:0 , PIN P3:0 , PIN P4:1
10ns	PIN P1:0 , PIN P2:1 , PIN P3:1 , PIN P4:0
15ns	PIN P1:0 , PIN P2:0 , PIN P3:0 , PIN P4:0
20ns	PIN P1:1 , PIN P2:1 , PIN P3:1 , PIN P4:1

FIG.2

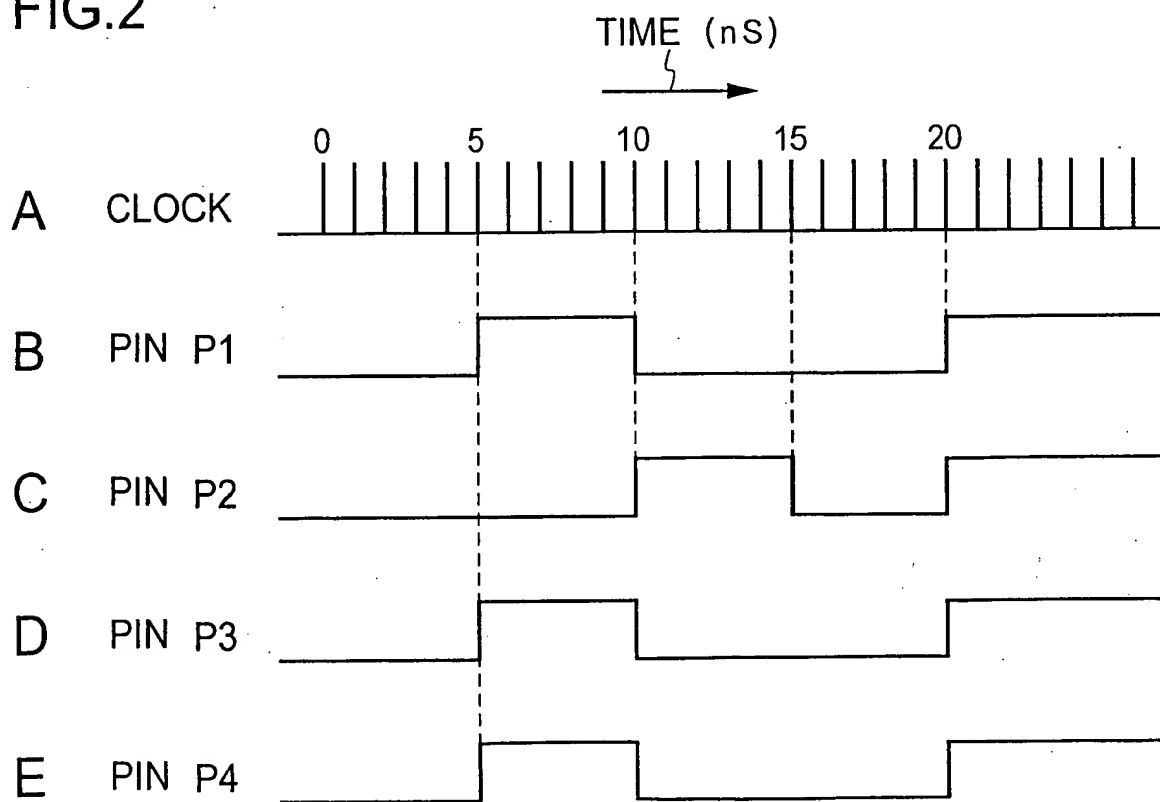


FIG.3

CYCLE BASIS FORMAT

TEST CYCLE (ADDRESS)	PIN No. P1	PIN No. P2	PIN No. P3	P4
1	TP:H T1:5ns T2:10ns	TP:L T1:5ns T2:10ns	TP:H T1:5ns T2:10ns	
2	TP:L T1:3ns T2:7ns	TP:H T1:5ns T2:10ns	TP:H T1:5ns T2:10ns	
	⋮	⋮	⋮	

FIG.4

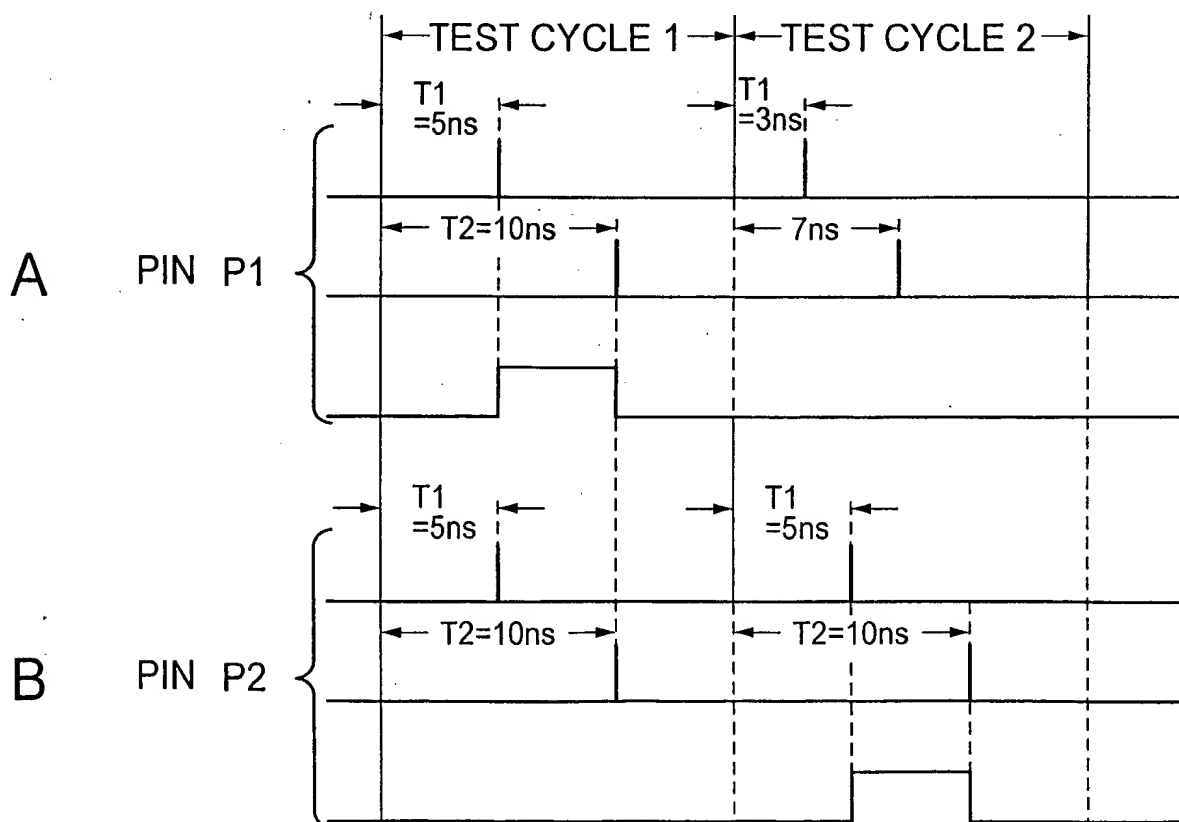


FIG.5 Prior Art

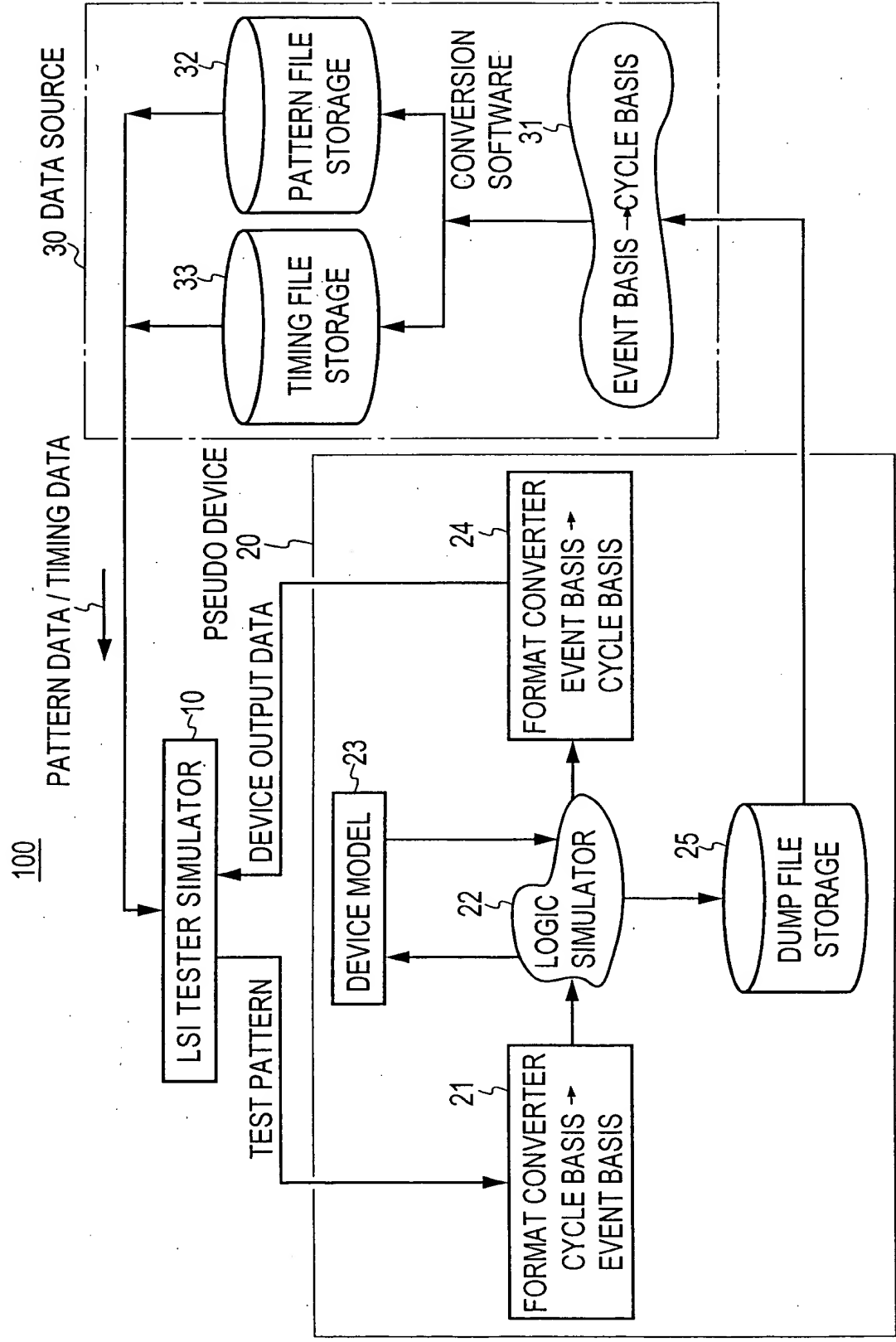


FIG.6

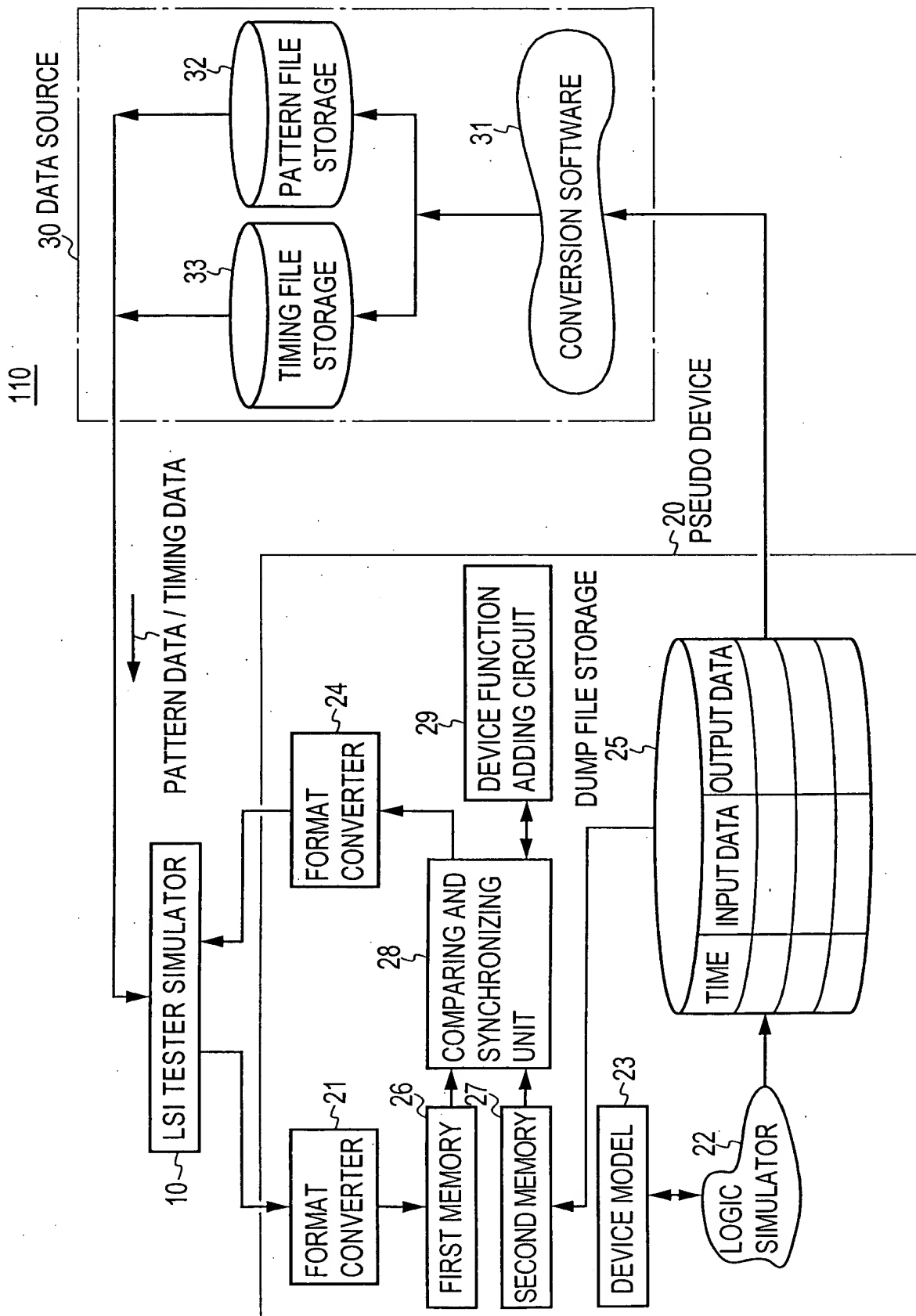


FIG.7

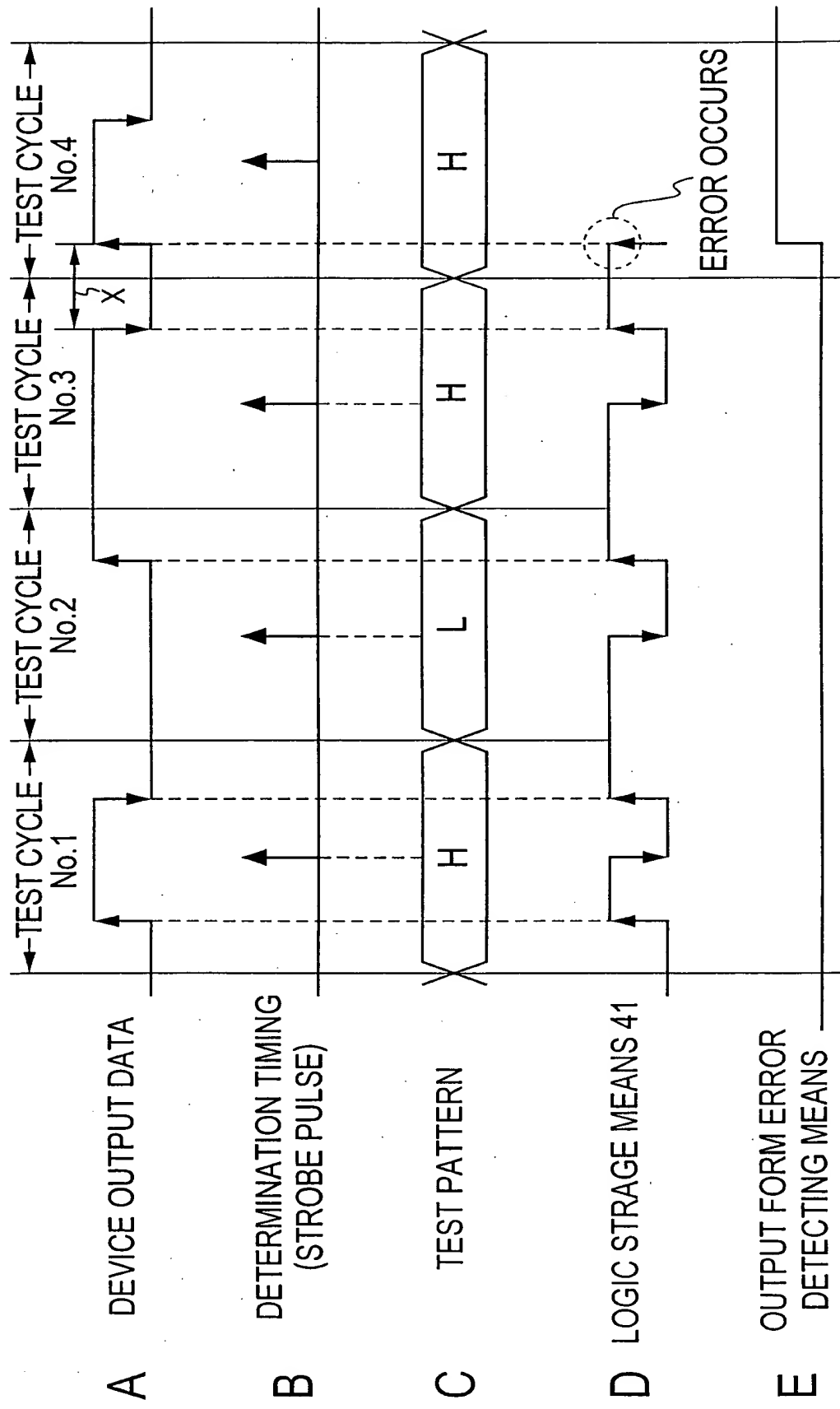


FIG.8

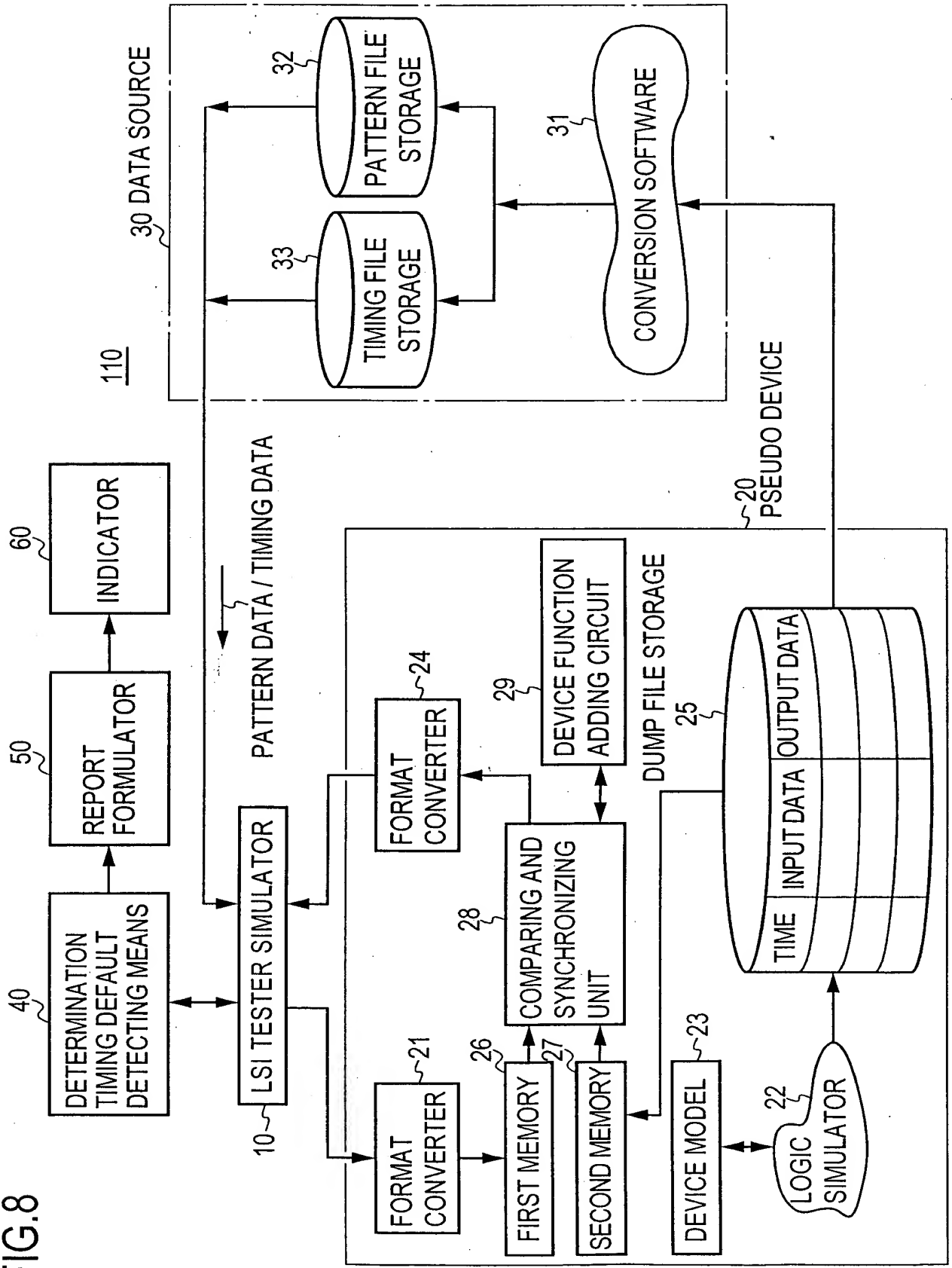


FIG.9

DETERMINATION TIMING
DEFAULT DETECTING MEANS

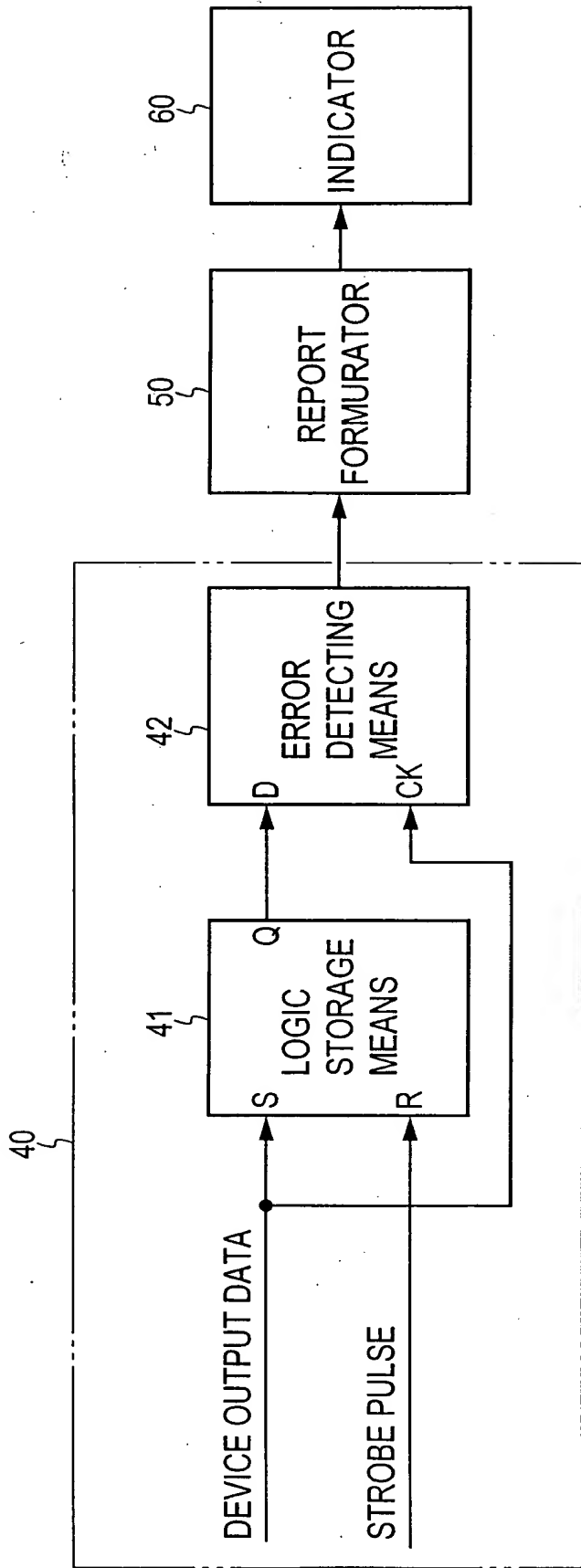


FIG.10

